IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/538,216	Confirmation No.	1792
Applicant	:	SCHMITZ, Jurriaan		
Filed	:	June 9, 2005		
TC/A.U.	:	2824		
Examiner	:	BERNSTEIN, Allison		
Docket No.	:	**NL02 1416 US**		
Customer No.	:	65913		

Title: : Vertical Insulated Gate Transistor and Manufacturing Method

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL RESPONSE & AMENDMENT

Sir:

In response to the Non-Final Office Action of March 23, 2007, please consider the following. Office Action had required a Drawing Amendment which had inadvertently left out in the previous response submitted June 28, 2007.

Amendments to the Specification there are no amendments in this paper.

Amendments to the Claims there are no amendments in this paper,

Amendments to the Drawings follow the Remarks/Arguments.

Remarks/Arguments begin on page 2 of this paper.